IN THE CLAIMS:

1. (Cancelled)

2. (Currently Amended) A ~~The~~ nonvolatile memory ~~according to claim 1,~~ comprising:

a plurality of memory cells, each of the memory cells having a first and a second source/drain areas, a control gate, and an insulating trap layer disposed between the control gate and a channel area lying between the first and the second source/drain areas, wherein

the trap layer includes a use bit area in proximity to the first source/drain area, for storing data depending on the presence or absence of electric charge to be trapped, and a non-use bit area in proximity to the second source/drain area, in which the electric charge is trapped while data is held in the use bit area, and

wherein at the time when an erasing operation mode for bringing the use bit area into an erased state is completed, or before a writing operation to the use bit area, the non-use bit area is put in the electric charge trapped state.

3. (Original) The nonvolatile memory according to claim 2, wherein in the erasing operation mode, both of the use bit area and the non-use bit area are put in the electric charge trapped state, and then, the use bit area of a plurality of memory cells is put in the erased state.

4. (Original) The nonvolatile memory according to claim 2, wherein in the erasing operation mode, both of the non-use bit area and the use bit area are put in the electric charge trapped state, and then, both the bit areas of a plurality of memory cells are put in the erased state, and further, the non-use bit area is put in the electric charge trapped state.

5. (Original) The nonvolatile memory according to claim 2, wherein in the erasing operation mode, both of the non-use bit area and the use bit area are put in the electric charge trapped state, and then, both the bit areas of a plurality of memory cells are put in the erased state, and wherein in the writing operation mode, the non-use bit area is put in the electric charge trapped state.

6. (Original) The nonvolatile memory according to claim 5, wherein in the writing operation mode, a writing pulse is applied to the non-use bit area, and the writing pulse is applied to the use bit area together with write verification for the use bit area.

7. (Original) The nonvolatile memory according to claim 5, wherein in the writing operation mode, the non-use bit area of the memory cell subject to writing is put in the electric charge trapped state whereas writing is not performed to the non-use bit area of the memory cell that is not subject to writing.

8. (Original) The nonvolatile memory according to claim 5, wherein in the writing operation mode, writing is performed to the use bit area after having put the non-use bit area in the electric charge trapped state.

9. (Cancelled)

10. (Currently Amended) The nonvolatile memory according to claim ~~9~~ 13, further comprising a use bit determining memory for determining which area of the trap layer is the use bit area, and wherein when the use bit area and the non-use bit area are switched, the data of the use bit determining memory is reversed.

11. (Original) The nonvolatile memory according to claim 10, wherein in an erasing operation mode, at least the non-use bit area is put in the erased state and the data of the use bit determining memory is rewritten.

12. (Original) The nonvolatile memory according to claim 10, wherein in at least one of the erasing operation mode, writing operation mode and read-out operation mode, the use bit area is determined depending on the data of the use bit determining memory.

13. (Currently Amended) A ~~The~~ nonvolatile memory ~~according to claim 9,~~ comprising:

a plurality of memory cells, each of the memory cells having a first and a second source/drain areas, a control gate, and an insulating trap layer disposed between the control gate and a channel area lying between the first and the second source/drain areas, wherein

the trap layer includes a use bit area disposed in proximity to one of the first and the second source/drain areas, the use bit area storing data depending on the presence or absence of electric charge to be trapped, and a non-use bit area disposed in proximity to the other of the first and the second source/drain areas, the non-use bit area being not in use for storing data, wherein

the use bit area and the non-use bit area of the trap layer are switched at every specified number of rewriting operations, and

wherein in the erasing operation mode, from the state where electric charge is trapped in the use bit area and the non-use bit area, new use bit areas of the plurality of memory cells are erased, and new non-use bit areas thereof are kept in the electric charge trapped state.

14. (Currently Amended) The nonvolatile memory according to claim ~~9~~ 13, wherein in the erasing operation mode, from the state where electric charge is trapped in the use bit area and the non-use bit area, both the bit areas of the plurality of memory cells are erased, and writing is performed to a new non-use bit area, for putting the new non-use bit area in the electric charge trapped state.

15. (Currently Amended) The nonvolatile memory according to claim ~~9~~ 13, wherein in the erasing operation mode, from the state where electric charge is trapped in the use bit area and the non-use bit area, both the bit areas of the plurality of memory cells are erased, and wherein in the writing operation mode, writing is performed to a new use bit area, for putting the new use bit area in the electric charge trapped state.

16. (Currently Amended) The nonvolatile memory according to claim ~~9~~ 13, wherein in the erasing operation mode, from the state where the electric charge is trapped in the use bit area, the use bit areas of the plurality of memory cells are erased.

17. (Currently Amended) The nonvolatile memory according to claim ~~9~~ 13, wherein in the erasing operation mode, from the state where the electric charge is trapped in the use bit area and the non-use bit area, both the bit areas of the plurality of memory cells are erased.

18. (Currently Amended) The nonvolatile memory according to claim 16 or 17, further comprising a use bit determining memory for ~~detemining~~ determining which area of the trap layer is the use bit area, and wherein in the erasing operation mode, the data of the use bit determining memory is reversed.